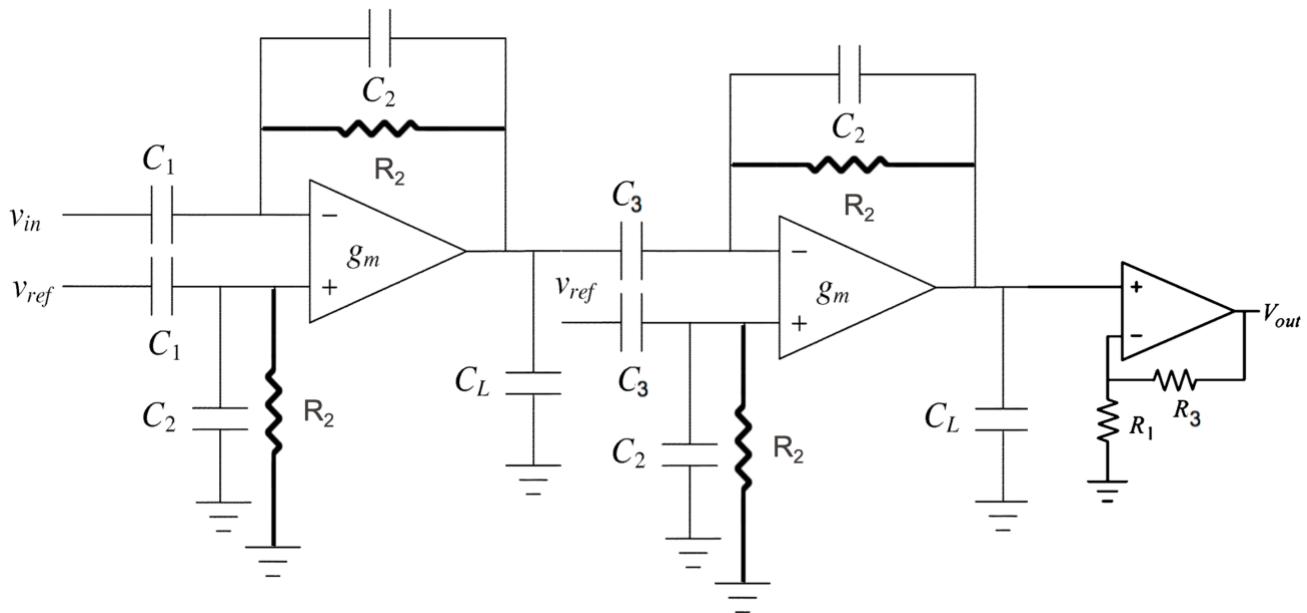


NX-422 Exercise 3, Implantable Electronics

1. (a) For the three-stage neural amplifier shown below, find the equation for the overall mid-band gain.

(b) Assuming $C_2 = C_u$ (unit capacitor), what are the values of C_1 and C_3 in terms of C_u that would result in a total mid-band gain of 1000 while minimizing the total capacitor in the circuit (and thus, the chip area)? You can ignore C_L in your calculations. Assume $R_1=40k\Omega$ and $R_3 = 60k\Omega$.

(c) If the amplifier's bandwidth is set by the first stage and $C_2 = 400\text{fF}$, what is the value of R_2 to pass signals in the LFP band (1-300Hz)?



2. Plot the drain current (I_D) of an NMOS as a function of V_{GS} as V_{GS} varies from 0 to 3V. Assume $W/L = 50/0.5$, $V_{DS} = 3V$, $V_{TH} = 0.7V$, and $\mu_n C_{ox} = 50\mu A/V^2$. What is the region of operation for the transistor? ($\lambda = 0$)

3. Draw the small-signal models of (a) a common-gate amplifier, and (b) a cascode amplifier shown below and find the voltage gain for each circuit.

